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(71) Applicant
Metscan Incorporated

(Incorporated in the USA - New York)

11450 Rochester Street, Lima, New York 14485, United States of America

(72) Inventor
Daniel H Hollands

(74) Agent and/or Address for Service
Urquhart-Dykes & Lord
91 Wimpole Street, London, W1M 8AH, United Kingdom

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G4A AKBX
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U1S S2146

(56) Documents cited
EP 0134966 A2 US 4897807 A US 4649373 A

(58) Field of search
UK CL (Edition L) G4A AKBX AKS
INT CL^5 G06F 1/32 3/00 3/02 3/023 3/05

(54) **Low power change-of-contact-state detector**

(57) A change of state detector 10' is provided that minimizes the amount of power required to monitor the state of one or more switches or contacts 20, 22. The number of components utilized is minimized to simplify the manufacturing process and reduce the expense of the detector. The detector supplies pulses to the or each contact to determine its state and compares the present state with the previous state as indicated by a signal from a dormant processor unit 16'. If the comparison shows a change of state, a wake-up signal is applied to the processor unit. The detector may be part of a gas meter, in which the processor unit counts actuations of contact 20 according to gas flow and reports the count over a communication link 18', anti-tamper contact 22 also being monitored. The comparison is effected using XOR logic (Figs 2, 5).

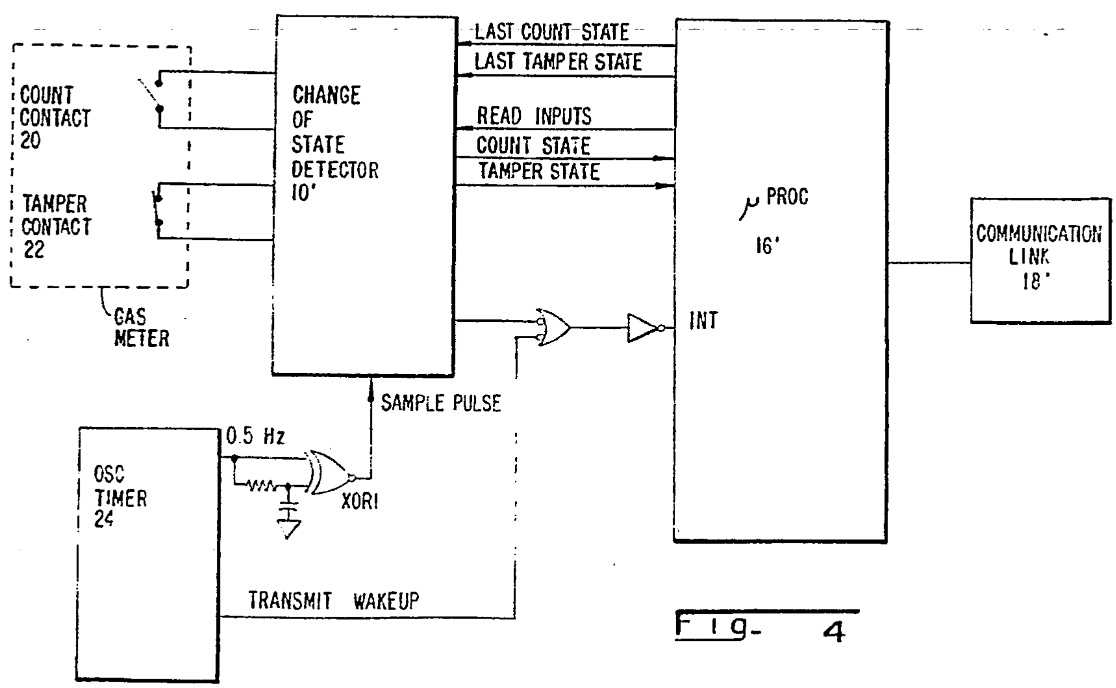

Fig- 4

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 262 172 A

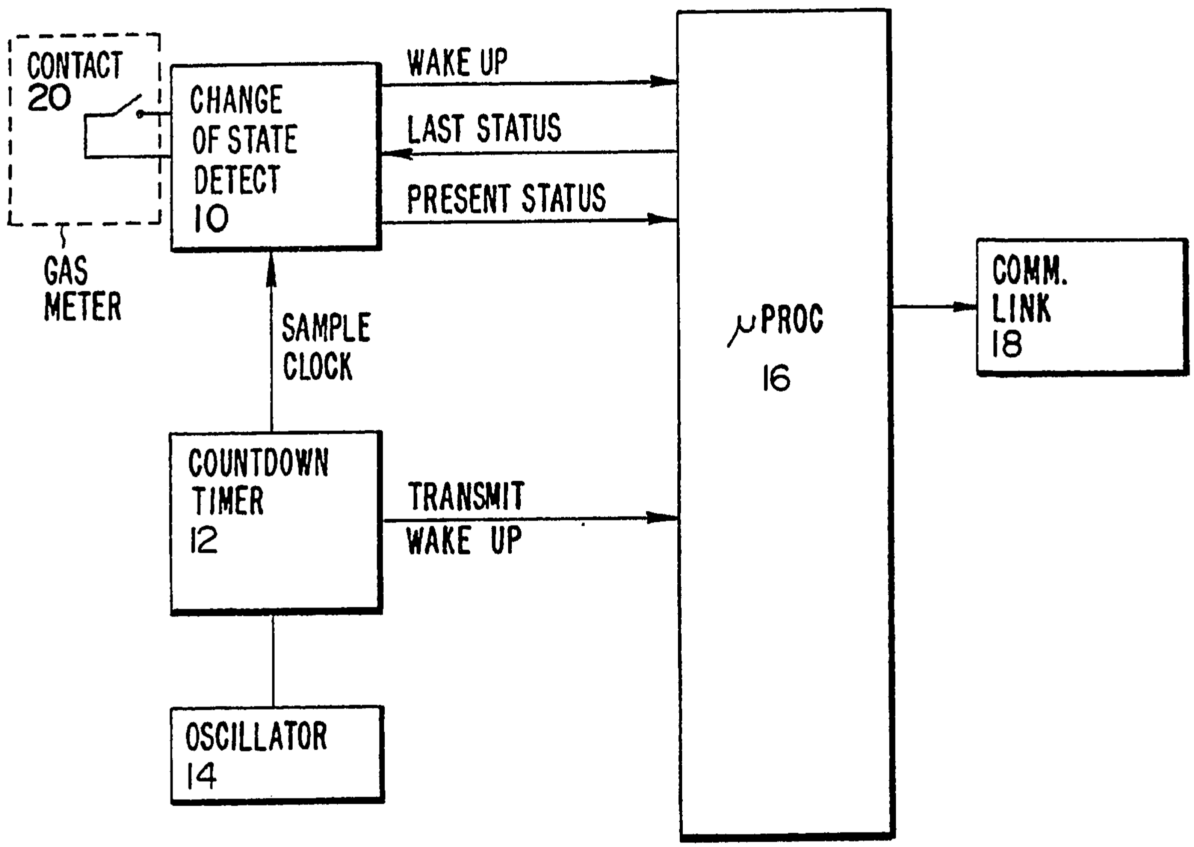
CONTACT
20
GAS
METER
CHANGE
OF STATE
DETECT
10
WAKE UP
LAST STATUS
PRESENT STATUS
SAMPLE
CLOCK
COUNTDOWN
TIMER
12
TRANSMIT
WAKE UP
OSCILLATOR
14
μPROC
16
COMM.
LINK
18

Fig. 1

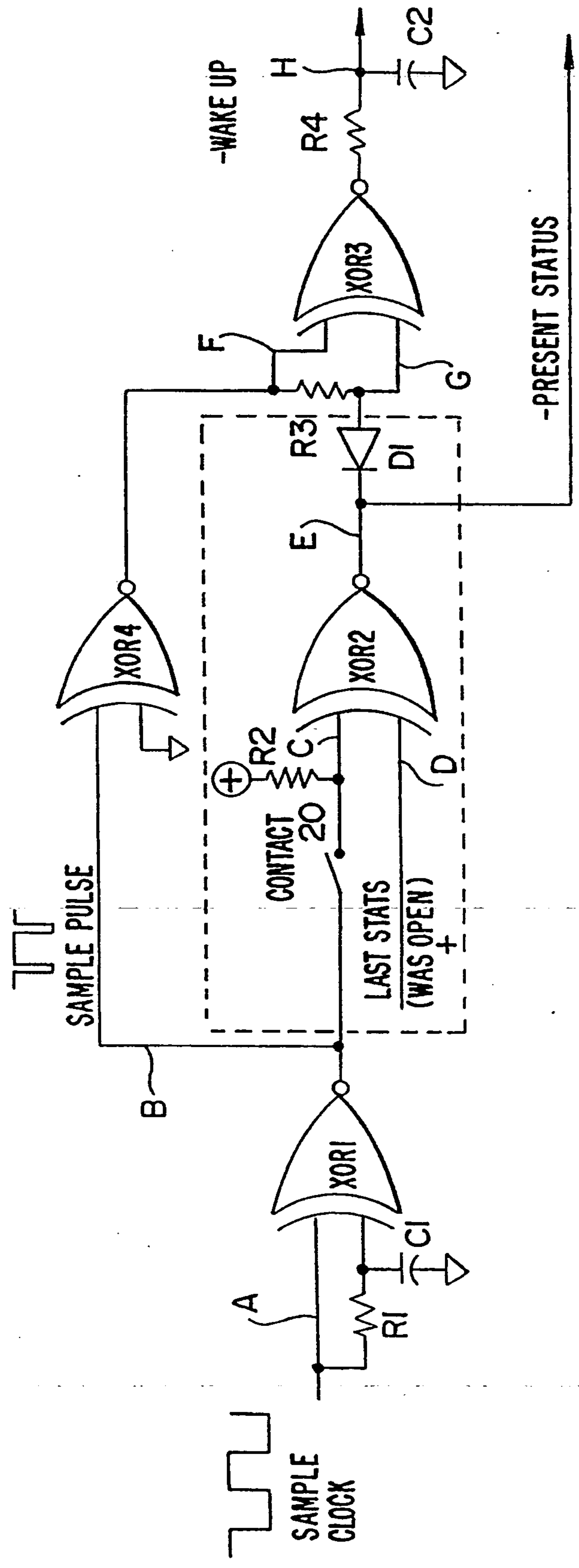
-WAKE UP
H
C2
R4
XOR3
F
G
-PRESENT STATUS
R3
D1
E
XOR4
XOR2
R2
C
D
CONTACT
20
LAST STATS
(WAS OPEN)
+
SAMPLE PULSE
B
XOR1
C1
A
R1
SAMPLE
CLOCK

Fig- 2

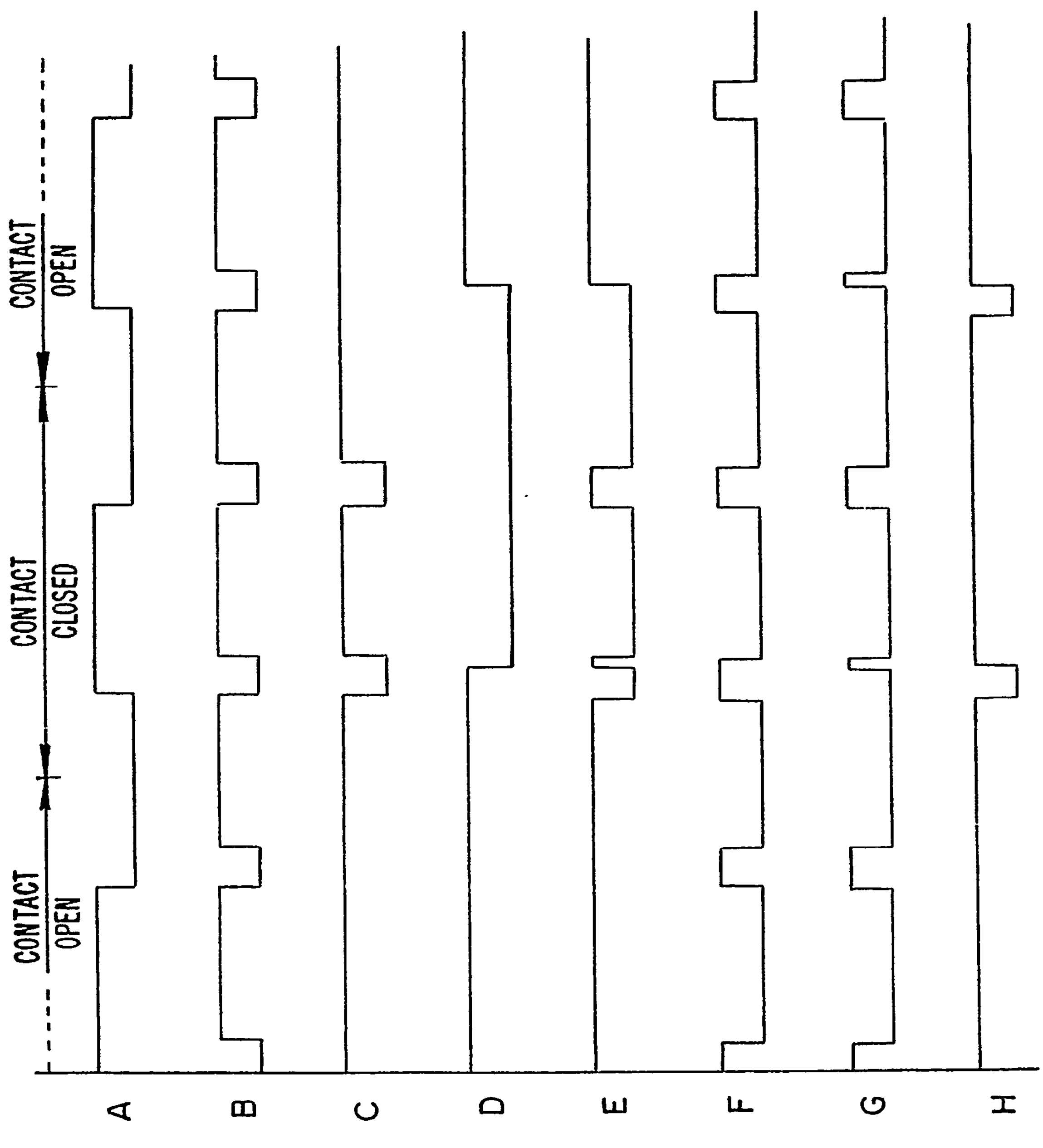

Fig_ 3

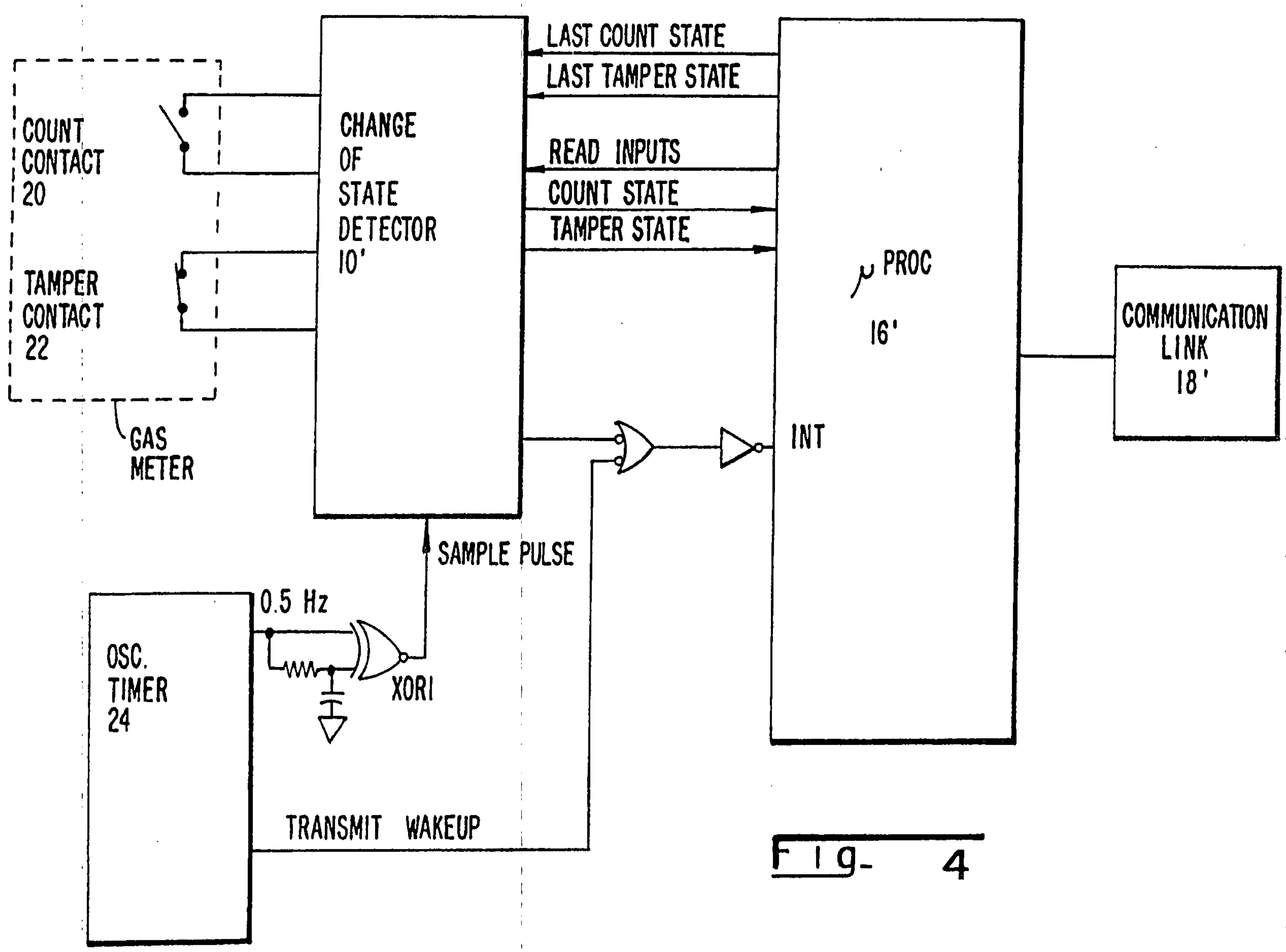
COUNT CONTACT 20
TAMPER CONTACT 22
GAS METER
CHANGE OF STATE DETECTOR 10'
LAST COUNT STATE
LAST TAMPER STATE
READ INPUTS
COUNT STATE
TAMPER STATE
μ PROC 16'
INT
COMMUNICATION LINK 18'
SAMPLE PULSE
0.5 Hz
XOR1
OSC. TIMER 24
TRANSMIT WAKEUP

Fig. 4

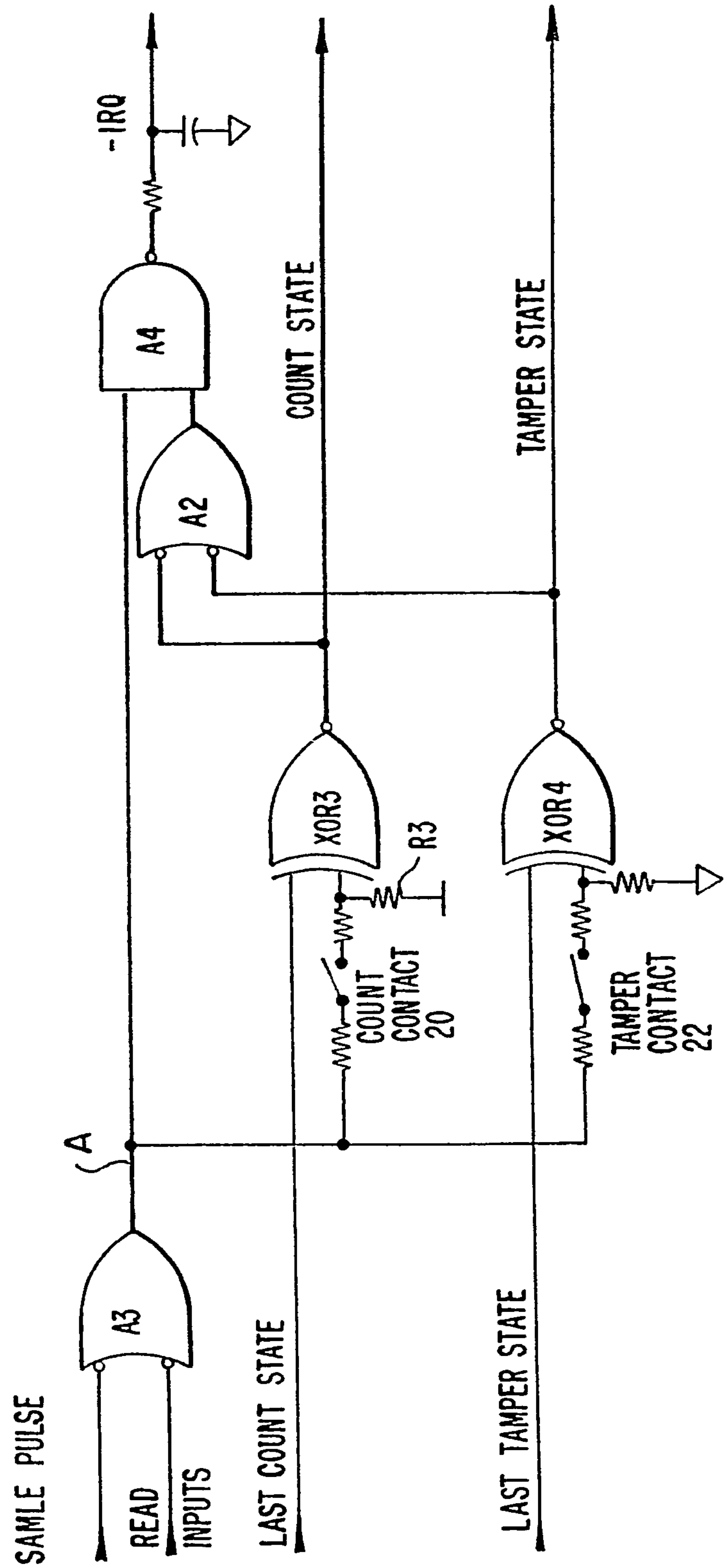
SAMLE PULSE
READ
INPUTS
A3
A
LAST COUNT STATE
LAST TAMPER STATE
XOR3
R3
COUNT
CONTACT
20
XOR4
TAMPER
CONTACT
22
A2
A4
-IRQ
COUNT STATE
TAMPER STATE

Fig- 5

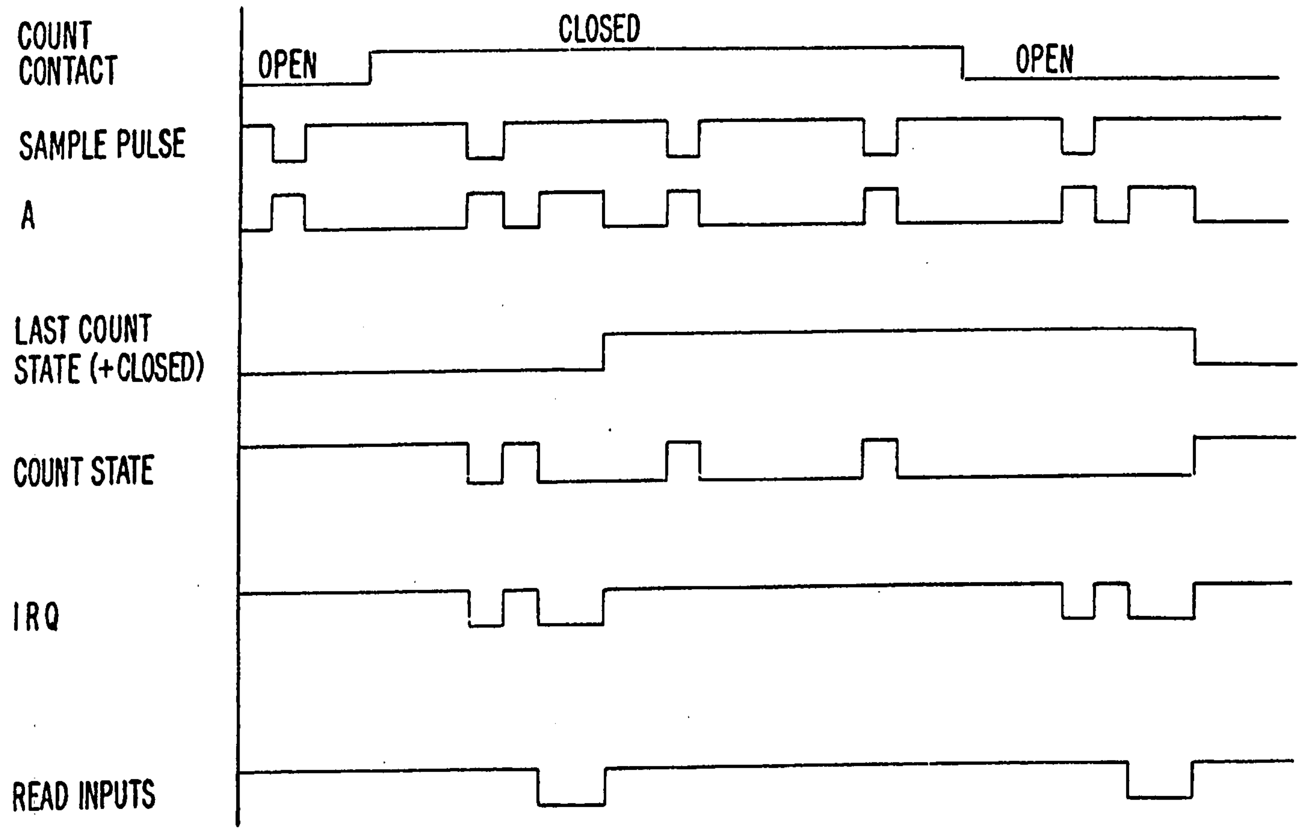
COUNT CONTACT
OPEN
CLOSED
OPEN
SAMPLE PULSE
A
LAST COUNT STATE (+CLOSED)
COUNT STATE
IRQ
READ INPUTS

Fig. 6

LOW POWER CONTACT CHANGE OF STATE DETECTOR

Field of the Invention

The invention relates in general to devices that detect changes in state of one or more switches or contacts. More specifically, the invention is related to a contact change of state detector that reduces the amount of power required to monitor the status of the switches or contacts.

Background of the Invention

There are a variety of systems that require the state of one or more switches or contacts to be monitored over an extended period of time. These systems typical utilize a central processing unit, for example a microprocessor, to periodically monitor the status of the switches by a polling process to detect a change in the state of the switch --from "on to off" or from "off to on"-- and implement a predetermined action in response to the state change. The polling process, however, reduces the operating efficiency of the central processing unit by reducing the amount of processing time available to perform other tasks. The process can also waste power if the central processing unit completes all required tasks and must remain active to simply perform the function of polling the switches.

An alternative to central processor polling is to include a separate switch monitoring circuit to monitor the state of the switches. The switch monitoring circuit can then generate and supply an interrupt signal to the central processor unit when a change of state is detected. The central processor unit services the interrupt request and then returns to other tasks while the switch monitoring circuit resumes monitoring the state of the switches. In order to conserve power, the central processor unit can enter a wait state when all

required tasks have been completed and remain in the wait state until a further interrupt signal is generated by the switch monitoring circuit. An example of a system that employs a switch monitoring circuit is illustrated in U.S. Patent 4,897,807.

While the placing of the central processor unit in a wait state can significantly reduce the amount of power required in the system, the switch monitoring circuit may also consume an undesirable amount of power for certain applications. It is therefore an object of the invention to provide a contact change of state detector, with a minimum number of components, that further reduces the amount of power required to monitor the status of one or more switches or contacts.

Summary of the Invention

A contact change of state detector is provided that minimizes the amount of power required to monitor the state of one or more switches or contacts. The number of components utilized in the change of state detector is minimized to simplify the manufacturing process and reduce the expense of the detector.

More specifically, a change of state detector is provided that includes a mechanism for generating a sample pulse signal; a mechanism for applying the sample pulse signal to at least one contact to be monitored to generate a signal indicative of the state of the contact; a comparitor coupled to the contact and to a processor unit, wherein the comparitor compares the signal indicative of the state of the contact to a signal received from the processor unit that is indicative of a last state of the contact and generates a signal indicative of whether a change in the state of the contact has occurred; and a mechanism for generating a wake up signal that is supplied to the processor unit in

response to the signal generated by the comparitor and the sample pulse signal.

Brief Description of the Drawings

With the above as background, reference should now be made to the following detailed description of the preferred embodiments and the accompanying drawings wherein:

Fig. 1 is a block diagram of a monitoring system incorporating a change of state detector in accordance with the present invention;

Fig. 2 is a schematic diagram of the change of state detector illustrated in Fig. 1;

Fig. 3 is a timing diagram illustrating the operation of the change of state detector illustrated in Fig. 2;

Fig. 4 is a block diagram of a second monitoring system incorporating a second embodiment of a change of state detector in accordance with the present invention;

Fig. 5 is a schematic diagram of the change of state detector illustrated in Fig. 4; and

Fig. 6 is a timing diagram illustrating the operation of the change of state detector illustrated in Fig. 4.

Detailed Description of the Preferred Embodiments

The invention will be described with reference to its implementation in gas line metering equipment. It will be understood, however, that the invention is not limited to the specific application set forth below.

Referring now to Fig. 1, a monitoring system for automatically reporting the amount of gas passing through a gas line is shown including a change of state detector 10, a countdown timer 12, an oscillator 14, a microprocessor 16, and a communications link 18. The

change of state detector 10 is used to monitor the status of a contact 20 coupled thereto. The contact 20 is incorporated in a gas line meter attached to a gas line and is activated each time a predetermined amount of gas has been metered.

The illustrated monitoring system is designed to count the number of times contact 20 is activated and to periodically report the count to a central location via the communication link 18. In operation, the oscillator 14 supplies a clock signal to the countdown timer 12. The countdown timer 12 is used to generated a SAMPLE CLOCK signal that is supplied to the change of state detector 10. The change of state detector 10, in response to the SAMPLE CLOCK signal, periodically checks the status of the contact 20 and compares the present status of the contact 20 with a LAST STATUS signal previously latched by the microprocessor 16. It should be noted that the microprocessor 16 is in a halt or wait state at this point to reduce the power requirements of the system. The change of state detector 10 generates and supplies a WAKE UP signal to the microprocessor 16 if the result of the comparison indicates that the contact 20 has changed state. The change of state detector 10 also supplies a PRESENT STATUS signal to the microprocessor 16 that is indicative of the present state of the contact 20. The microprocessor 16, in response to the WAKE UP signal, reads the PRESENT STATUS signal, increments a gas count register if appropriate, changes the LAST STATUS to equal the PRESENT STATUS signal, and then returns to the wait state until a subsequent WAKE UP signal is generated by the change of state detector 10. The countdown timer 12 also generates and supplies a TRANSMIT WAKEUP signal to the microprocessor 16 at least once a day. The microprocessor 16 activates the communications link 18 in response to the TRANSMIT WAKEUP

signal and transmits the count contained in the gas count register to a central location either by radio communication or by a hard-wired link. The microprocessor 16 then resets the gas count register and enters the wait state until a subsequent WAKEUP or TRANSMIT WAKEUP signal is received. Thus, the microprocessor 16 is only active for the time necessary to act on the change in state of the contact 20 and to transmit the accumulated count to the central location via the communications link 18.

Fig. 2 is a schematic diagram of the change of state detector 10. An exclusive OR gate XOR1 is used to generate a logic low level SAMPLE PULSE signal from the SAMPLE CLOCK signal supplied by the countdown timer 12. The SAMPLE PULSE signal is of a pulse width long enough, typically about 10 ms, to wake up the microprocessor 16 and to give the microprocessor 16 sufficient time to check the PRESENT STATUS signal. It should also be noted that the SAMPLE PULSE signal can be directly generated by the countdown timer 12 if desired. The output of the exclusive OR gate XOR1 is coupled to contact 20, which in turn is connected to a first input of a second exclusive OR gate XOR2 and an invertor implemented by exclusive OR gate XOR4. The first input of the exclusive OR gate XOR2 is also coupled to a logic high voltage source via a pull-up resistor R2. A second input of the second exclusive OR gate XOR2 is coupled to receive the LAST STATUS signal from the microprocessor 16. The outputs from the exclusive OR gates XOR4 and XOR2 are connected to an AND gate implemented through the use of exclusive OR gate XOR3, resistor R3 and diode D1.

In operation, the first input of the exclusive OR gate XOR2 is held at a logic high level via the pull-up resistor R2 if the contact 20 is open (See Fig. 3). If the LAST STATUS signal is at a high logic level signal,

the output of the exclusive OR gate XOR2 will remain at a low logic level as both inputs to the gate are equal. Thus, the high logic level signal generated by the exclusive OR gate XOR4, in response to the SAMPLE PULSE signal, and the low logic level signal generated by the exclusive OR gate XOR2 will cause the output of the exclusive OR gate XOR3 to remain at a low logic level. When the contact 20 closes, however, the first input of the exclusive OR gate XOR2 is brought to a logic low level via the exclusive OR gate XOR1 for the duration of the SAMPLE PULSE, i.e., the application of the SAMPLE PULSE to the contact 20 causes the signal "C" which is indicative of the state of the contact 20 and applied to the first input of the exclusive OR gate to go to a logic low level. The difference between the first and second inputs of the exclusive OR gate XOR2 causes the output of the gate to go to a logic high level which, in combination with the high logic level signal generated by the exclusive OR gate XOR4, causes the output of the exclusive OR gate XOR3 to go to a high logic level for the duration of the SAMPLE PULSE signal. Thus, the exclusive OR gate XOR3 generates the WAKE UP signal that is supplied to the microprocessor 16 when a change in the state of contact 20 occurs.

The change of state detector 10 illustrated in Fig. 2 is used to monitor the condition of a signal contact. It will be understood, however, that the same basic circuit configuration can be used to monitor a plurality of contacts by duplicating the comparison circuitry located within the dotted line of Fig. 2 for each contact and coupling the duplicated circuitry to the input of the exclusive OR gate XOR3 at point "G" as shown in the drawing.

A second monitoring system incorporating a second embodiment of the change of state detector 10' coupled to

a count contact 20 and a tamper contact 22 is shown in Fig. 4. The tamper contact 22 is used to generate a signal indicative of whether an individual has attempted to tamper with the gas meter. The change of state detector 10' is coupled to a microprocessor 16' and an oscillator timer circuit 24. The oscillator timer circuit 24 generates a 0.5 Hz clock signal that is supplied to an exclusive OR gate XOR1 to generate a one pulse per second SAMPLE PULSE signal. The oscillator timer circuit 24 also generates a TRANSMIT WAKEUP signal that is supplied to the microprocessor 16'.

In the change of state detector 10' illustrated in Fig. 5, the low level SAMPLE PULSE signal is supplied to a first input of an OR gate A3. A second input of the OR gate A3 is coupled to receive a READ INPUT signal from the microprocessor 16'. The output of the gate A3 is coupled to the contacts to be tested, namely the count contact 20 and the tamper contact 22, and to a first input of an AND gate A4. Each contact is connected to a first input of a corresponding exclusive OR gate (XOR3 and XOR4) which is also coupled to ground through a pull-down resistor (for example R3). The second input of each exclusive OR gate is coupled to receive a last state signal (LAST COUNT STATE and LAST TAMPER STATE) that corresponds to the contact coupled to the first input of the gate. The outputs of the exclusive OR gates are supplied to an OR gate A2 which has its output connected to a second input of the gate A4.

In operation, the READ INPUT signal is normally held at a high logic level. The output of the gate A3 (point "A") is therefore the inverse of the SAMPLE PULSE signal. Assuming that the last state of the contacts was closed, the LAST COUNT STATE signal and the LAST TAMPER STATE signal are held at a logic high level. If the count contact 20 opens and the tamper contact 22 remains

closed, the signal applied to the first input of the exclusive OR gate XOR4 will be pulled high by the output of gate A3 for the duration of the SAMPLE PULSE signal and the signal applied to the first input of the exclusive OR gate XOR3 will be pulled low via resistor R3. As a result, the output of the exclusive OR gate XOR3 will go high as the two inputs to the gate are unequal while the output of exclusive OR gate XOR4 will go low as the two inputs to the gate are equal. The high output signal from the exclusive OR gate XOR3 will cause the output of the OR gate A2 to go to a logic high level. Thus, the output of NAND gate A4 will go low for the duration of the SAMPLE PULSE SIGNAL to generate a wake up or interrupt request signal pulse IRQ. Once the interrupt pulse is generated, the microprocessor 16' places the READ INPUTS signal at a logic low level for a time sufficient to check the COUNT STATE and TAMPER STATE signals and to adjust the LAST COUNT STATE (goes low to indicate that the count contact 20 opened) signal and the LAST TAMPER STATE signal. Fig. 6 is a timing diagram illustrating the operation of the change of state detector 10'.

The provision of the READ INPUTS signal allows the microprocessor 16' to maintain the operation of the circuit for as long as is necessary to complete the reading of the COUNT STATE signal and the TAMPER STATE signal. The pulse width of the SAMPLING PULSE can therefore be reduced, as the width of the SAMPLING PULSE does not control how long the microprocessor 16' will have access to the signals indicative of the present status of the contacts to be monitored.

The invention has been described with reference to certain preferred embodiments thereof. It will be understood, however, that modification and variations can be made within the scope of the appended claims.

WHAT IS CLAIMED:

1. A change of state detector comprising: means for generating a sample pulse signal; means for applying the sample pulse signal to at least one contact to be monitored to generate a signal indicative of the state of the contact; comparison means coupled to the contact and to a processor unit, wherein the comparison means compares the signal indicative of the state of the contact to a signal received from the processor unit that is indicative of a last state of the contact and generates a signal indicative of whether a change in the state of the contact has occurred; and means for generating a wake up signal that is supplied to the processor unit in response to the signal generated by the comparison means and the sample pulse signal.

2. A change of state detector as claimed in claim 1, wherein the comparison means comprises an exclusive OR gate.

3. A change of state detector as claimed in claim 1, wherein the means for generating a wake up signal includes means for inverting the sample pulse signal and means for performing a logical AND operation on the inverted sample pulse signal and the signal generated by the comparison means.

4. A change of state detector as claimed in claim 1, wherein the means for generating a sample pulse signal includes an OR gate that is coupled to receive a read input signal from the processor unit and the sample pulse signal, and wherein the OR gate inverts the sample pulse signal before it is applied to the contact and the means for generating a wake up signal.

5. A change of state detector as claimed in claim 4, wherein the means for generating a wake up signal includes means for performing a logical NAND operation on the inverted sample pulse signal and the signal generated by the comparison means.

6. A change of state detector comprising: a first OR gate having a first input coupled to receive a sample pulse signal, a second input coupled to receive a read input signal from a processor unit, and an output coupled to a count contact and a tamper contact to be monitored; a first exclusive OR gate having a first input coupled to receive a last count state signal from the processor unit and a second input coupled to the count contact; a second exclusive OR gate having a first input coupled to receive a last tamper state signal from the processor unit and a second input coupled to the tamper contact; a second OR gate coupled to the outputs of the first and second exclusive OR gates; and a NAND gate coupled to the output of the first and second OR gates.

7. A system for monitoring the gas flow in a line comprising: a gas meter including a count contact and a tamper contact; a change of state detector coupled to the gas meter to monitor the state of the count contact and the tamper contact and generate a wake up signal when at least one of the count contact and the tamper contact change state; a timer/oscillator circuit coupled to the change of state detector; a processor unit coupled to the change of state detector, wherein the processor unit remains in a wait state until receipt of the wake up signal from the change of state detector; and a communications link coupled to the processor unit.

8. A system for monitoring the gas flow in a line as claimed in claim 7, wherein the change of state detector includes a first OR gate having a first input coupled to receive a sample pulse signal from the timer/oscillator circuit, a second input coupled to receive a read input signal from the processor unit, and an output coupled to the count contact and the tamper contact to be monitored; a first exclusive OR gate having a first input coupled to receive a last count state signal from the processor unit and a second input coupled to the count contact; a second exclusive OR gate having a first input coupled to receive a last tamper state signal from the processor unit and a second input coupled to the tamper contact; a second OR gate coupled to the outputs of the first and second exclusive OR gates; and a NAND gate coupled to the output of the first and second OR gates.

9. A change of state detector as claimed in either claim 1 or claim 6 and substantially as herein described with reference to the accompanying illustrative drawings.

10. A monitoring system substantially as herein described with reference to Figures 1 to 3 or with reference to Figures 4 to 6 of the accompanying illustrative drawings.

Patents Act 1977
Examiner's report to the Comptroller under S. ction 17 (The Search Report)

Application number
GB 9225137.0

Relevant Technical fields

(i) UK Cl (Edition L) G4A(AKBX,AKS)

(ii) Int Cl (Edition 5) G06F(1/32,3/00,3/02,3/023, 3/05)

Databases (see over)

(i) UK Patent Office

(ii)

Search Examiner

B G WESTERN

Date of Search

1 MARCH 1993

Documents considered relevant following a search in respect of claims 1-5,9,10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A,&	EP 0134966 A2 (IBM) see whole document	All
A,&	US 4649373 A (BLAND ET AL (IBM)) see whole document	All
A	US 4897807 A (OHSAWA (CANON)) see whole document	All

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

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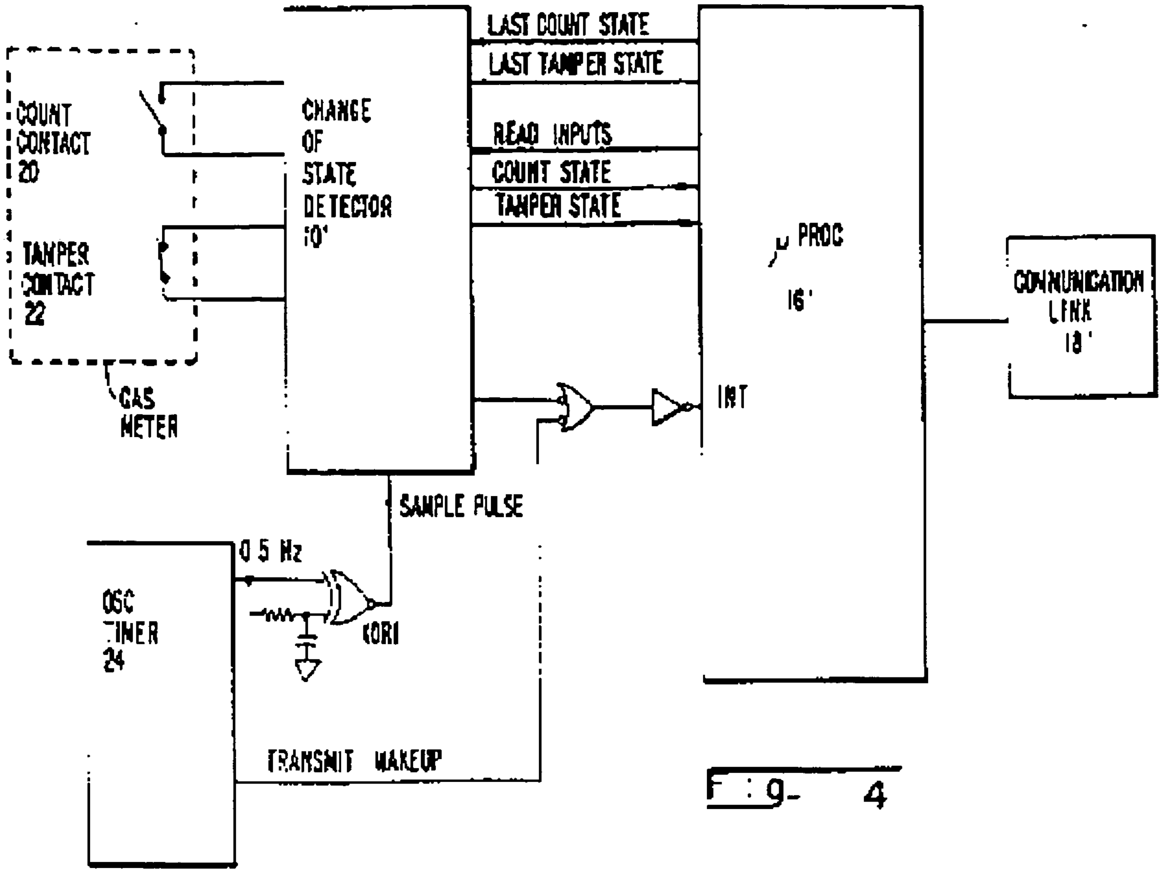
AN: PAT 1993-184731
TI: Low power change of contact detector relates to contact change of state detector that reduces amount of power required to monitor status of switches or contacts
PN: **GB2262172**-A
PD: 09.06.1993
AB: The change of state detector (10) minimises the amount of power required to monitor the state of one or more switches or contacts (20, 22). The number of components utilised is minimised to simplify the manufacturing process and reduce the expense of the detector. The detector supplies pulses to each contact to determine its state and compares the present state with the previous state as indicated by a signal from a dormant processor unit (16). If the comparison shows a change of state, a wake-up signal is applied to the processor unit. The detector may be part of a gas meter, in which the processor unit counts actuations of contact (20) according to gas flow and reports the count over a communication link (18), anti-tamper contact (22) also being monitored. The comparison is effected using XOR logic.; Simplifies manufacturing process. Reduces cost of detector.
PA: (METS-) METSCAN INC;
IN: HOLLANDS D H;
FA: **GB2262172**-A 09.06.1993;
CO: GB;
IC: G01F-001/00; G06F-001/32; G06F-003/00;
MC: S02-C01; T01-J08; X12-H03A;
DC: S02; T01; X12;
FN: 1993184731.gif
PR: US0801855 03.12.1991;
FP: 09.06.1993
UP: 09.06.1993


LAST COUNT STATE
LAST TAMPER STATE
COUNT CONTACT 20
CHANGE OF STATE DETECTOR 10'
READ INPUTS
COUNT STATE
TAMPER STATE
TAMPER CONTACT 22
μ PROC
16'
COMMUNICATION LINK 18'
GAS METER
INT
SAMPLE PULSE
0.5 Hz
OSC TIMER 24
XOR1
TRANSMIT WAKEUP

F:g- 4